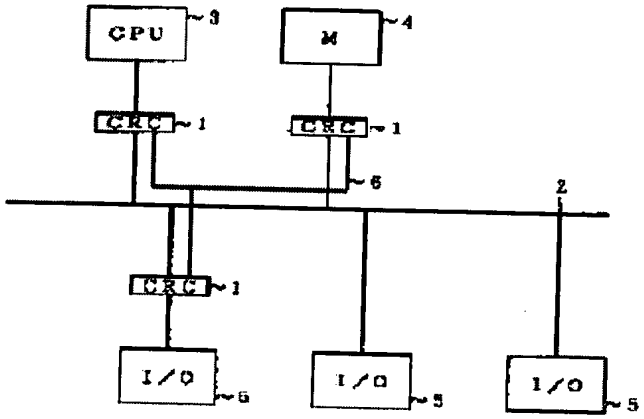
BUS COMMUNICATING MEANS

Publication number: JP6012269
Publication date: 1994-01-21
Inventor: IWATSUKI KAZUKO; ONISHI KATSUYOSHI; OGURA TOSHIHIKO; SHINOZAKI MASATSUGU
Applicant: HITACHI LTD
Classification:
- International: ***G06F11/00; G06F11/10; H04L12/40;*** **G06F11/00; G06F11/10; H04L12/40;** (IPC1-7): G06F11/00; G06F11/10; H04L12/40
- European:
Application number: JP19920167223 19920625
Priority number(s): JP19920167223 19920625

Abstract of **JP6012269**

PURPOSE:To construct a high-reliability system for handling a huge amount of data by adopting a bus provided with a CRC system as an error detecting means for improving the reliability of bus communication in a computer system. CONSTITUTION:The computer system using a standard bus, which is not provided with a parity bit system, uses an error controller 1 provided with a CRC code generator and an error detector used for a communication network as the error detecting means. When a CPU 3, main storage device 4 and input/ output device 5 respectively output data as bus masters, the data are not directly outputted to a standard bus 2 but outputted to the standard bus 2 after adding a CRC code through the error controller 1. When transfer is started, at the same time, the error controller 1 confirms it through an exclusive bus 6 whether the error controller 1 is also installed at the receiving destination or not and when it is installed, it is informed of the error controller at the opposite side through the exclusive bus 6 that the CRC code is added behind the transfer data.



Japanese Patent Application Laid-Open No. H6-12269 (Reference 3)

(54) [Title of the Invention]

BUS COMMUNICATING MEANS

(57) [Abstract]

[Object]

To construct a high-reliability system for handling an enormous amount of data by adopting a bus provided with a CRC method as error detecting means for improving the reliability of bus communication in a computer system.

[Constitution]

Figure 1 shows an example of configuration of a computer system having a highly reliable bus communication means using a standard bus. In Figure 1, reference numeral 1 denotes an error control device with a CRC code generator and an error detector; 2, standard bus without a parity bit method; 3, CPU managing the entire system; 4, main storage; 5, input-output device; and 6, dedicated bus to which only error control device 1 is connected.

[Claims for the Patent]

[Claim 1]

Bus communication means in a computer system having a parallel bus transferring a plurality of bits at a time characterized by comprising error detection means by a CRC method.

[Claim 2]

A computer system characterized by comprising the bus communication means according to claim 1.

[Claim 3]

The error detection control device according to claim 1, characterized by comprising:

a CRC code generating operation circuit;

a CRC code error detecting means;

a control signal generating means on the bus; and

a dedicated communication means for mutual communication interposed between the parallel bus transferring a plurality of bits at a time and devices which can be connected to the bus.

[Claim 4]

The device having a function of error detection control according to claim 1, characterized by comprising:

a CRC code generating operation circuit;

a CRC code error detecting means;

a control signal generating means on the bus; and

a dedicated communication means for mutual communication connected to the parallel bus without the function of error detection by a CRC code .

[Claim 5]

The bus communication means according to claim 1, wherein a CRC code equal in bit number to the bit width of the bus is transferred at a time on the parallel bus.

[Claim 6]

The bus communication means according to claim 1, wherein a CRC code greater in bit number than the bit width of the bus is transferred plural times on the parallel bus.

[Detailed Description of the Invention]

[0001]

[Industrial Application Field]

The present invention relates to the bus communication means of a high reliability system, and in particular, to the bus communication means of a highly reliable system using a CRC method.

[0002]

[Conventional Art]

A main storage is regarded as relatively low in reliability among composing elements of a general computer system. For this reason, a bus with a parity bit as shown in Figure 2 has been developed to increase reliability in bus communication in the system and actually there has been a system with a main storage and a device accessing thereto provided with functions for parity generation and parity check. For example, Japanese Patent Laid-Open No. 60-251442 describes a parity circuit for a bidirectional bus as a means of realizing a bus with a parity bit.

[0003]

On the other hand, a CRC method other than the above parity bit method has been frequently used as error detecting means to improve reliability in communication between systems such as local area network (LAN).

[0004]

In the CRC method, if a polynomial G(x) for generating CRC codes is set to g degree, a data M(X) is shifted by g bits to a higher degree side and divided by G(X). Then, the remainder R(X) is added to the data as a check bit and transmitted. If a transmission data F(X) is represented by the following equation,

[0005]

[Formula 1]

$$F(X) = X^{g} \cdot M(X) + R(X)$$

[0006]

F(X) can be divided by G(X), so that a receiving side divides F(X) by G(X), and if F(X) cannot be divided by G(X), it can be determined that an error exists. The division used herein is modulo 2 arithmetic (EX-OR operation).

[0007]

Figure 3 shows an example of an actualized CRC. Reference numeral 11 denotes a shift register; 12, EX-OR processor; and 13, a changeover switch for switching operation output results to destination. First, the data M(X) starts to be transmitted from a higher degree as the transmission data F(X) and is input into the EX-OR processor 12. The changeover switch 13 is thrown to a remainder calculation position. The shift register 11 is cleared to zero prior to input. When the data is shifted to the right every time the data is input bit by bit, the remainder R(X) is set to the shift register 11 after the least significant bit of data M(X) has been input. At this point, the changeover switch 13 is thrown to remainder output position to transmit the remainder R(X) following the data M(X). A receiving side has the same device to sequentially receive the transmission data F(X). If the data does not include an error, the contents of the shift register 11 are zero in all bits after the least significant bit of F(X) has been input.

[0008]

When the CRC is practically used in communication network, a certain fixed value is set in advance to the shift register 11 to prevent

the influence of other errors to determine whether the content of the shift register 11 is set to a certain fixed value after processing has been terminated.

[0009]

[Problems to be Solved by the Invention]

In bus communication in a conventional computer system, interest mainly has centered on a single transfer, so that a parity bit method has been considered enough as a means of improving reliability. However, recent computer systems performing a sophisticated image processing and being incorporated into communication network frequently transfer a large amount of data at a time in the system.

[0010]

A bus is required which is equipped with a method higher in error detection capability than a conventional parity bit to achieve a high reliability even when an enormous amount of data is thus transferred at a time.

[0011]

On the other hand, a standard bus which does not have even a parity bit method for reasons of cost, performance and versatility can be used in a computer system from which high reliability is demanded. An EISA bus is an example of a standard bus which does not have the parity bit method. In this case, means is required for improving reliability in bus communication without the influence of the specifications of the bus.

[0012]

The present invention has for its purpose to realize a parallel bus provided with the CRC method used in communication network as a means of improving reliability in bus communication in a computer system,

thereby enabling a highly reliable system capable of handling an enormous amount of data to be constructed.

[0013]

[Means for Solving the Problems]

The present invention provides a parallel bus into which the CRC method is incorporated as an error control system to achieve the above purpose.

[0014]

In addition, an error control device with a CRC code generator and an error detector is interposed between a standard bus which does not have a parity bit method and the adapters and memories which are attached to the standard bus to add CRC codes to the end of data transmission to detect errors, thereby realizing bus communication means capable of detecting errors.

[0015]

[Operation]

The computer system including the bus communication means according to the present invention can achieve high reliability even for cases where an enormous amount of data is handled.

[0016]

Furthermore, the error control device with the CRC code generator and the error detector is interposed between the standard bus and the adapters and memories which are attached to the standard bus to add CRC codes to the end of the data transmission to detect errors, which allows the construction of a highly reliable system to which many versatile adaptors of the standard bus are made available.

[0017]

According to the present invention, the adoption of the CRC method achieves reliability described below.

[0018]

(1) Odd numbers of errors in transmission data are all detected.

[0019]

(2) When the polynomial G(X) for generating CRC codes is set to g degree, error data groups which are g degree or less in length are all detected.

[0020]

(3) When the quantity of transmission data is the (g - 1) power of 2 or less, errors of two bits or less are all detected.

[0021]

[Embodiments]

The embodiment of the present invention is described below with reference to the drawings.

[0022]

Figure 1 is an example of configuration of the computer system with highly reliable bus communication means using the standard bus according to the embodiment of the present invention. In the figure, reference number 1 denotes an error control device with the CRC code generator and the error detector; 2, standard bus without the parity bit method; 3, CPU managing the entire system; 4, main storage; 5, input-output device; and 6, dedicated bus connected only to the error control device 1. Figure 4 shows one example of the functional block diagram of the error control device 1.

[0023]

A description is made below of the bus communication means using the error control device 1 and communication means among the error control device 1, CPU 3, main storage 4 and input-output devices 5.

[0024]

When the CPU 3, main storage 4 and input-output devices 5 placing the error control devices 1 between the standard bus and those units output data as a bus master, those units output data not directly to the standard bus 2 but to the error control device 1 to add the CRC code to data therein and transmit it to the bus 2. The error control device 1 confirms if the error control device 1 is also placed at the receiving side through the dedicated bus 6 at the same time of transmission start. When the error control device 1 is placed there, the error control device 1 notifies the error control device 1 on the receiving side of the CRC code being added to the end of transfer data through the dedicated bus 6.

[0025]

The error control device 1 on the receiving side as a bus slave outputs received data to the device on the receiving side and at the same time performs an error detection processing and causes the sending and the receiving end to wait for the termination of transfer using means provided with the standard bus 2 until the error detection processing is terminated. If no error is found, transfer is terminated without doing anything. If an error is found in received data, an error report signal provided on the standard bus 2 is sent to the sending and the receiving end and then transfer is terminated.

[0026]

When the CPU 3 or the bus masters inquire of the device on the receiving side about the output of the error report signal, the error control device 1 sends detailed information on error to the CPU 3 or the bus masters in place of the device on the receiving side.

[0027]

The same processing is performed also when the bus mater receives data. If an error is detected, the error control device 1 attached to the bus master sends detailed information on the error to the CPU 3 or the bus masters.

[0028]

On the other hand, when the error control device 1 is not attached to the bus slave, the error control device 1 of the bus master does nothing. Similarly, the error control device 1 on the bus slave side received transfer from the bus mater without the error control device 1 does not perform error detection because there is no communication from the error control device 1 of the bus master.

[0029]

Figure 4 describes how the aforementioned processing is performed in the error control device 1. Here, reference numeral 22 denotes a data line out of the signal lines of the standard bus 2; 23, signal line except the data line in the standard bus 2; 24, ALU realized by the configuration of an operation circuit depending on generator polynomial G(X); 25, register to which the remainder equation R(X) is set; 26, error control device controlling section for controlling the functions in the error control circuit 1; 27, bus control signal generating section for controlling the output timing of control signal of the standard bus when data with the CRC code is transferred; and

28, control signal generating section dedicated for CRC error detection which processes signal line of the dedicated bus 6.

[0030]

A bus in a computer system is a parallel bus with a data width of typically 16 bits or 32 bits. For this reason, the CRC circuit for a serial bus used in the communication network shown in Figure 3 is extended to be used as a parallel bus, thereby realizing the CRC circuit for operating parallel data at a time. The ALU 24 is an arithmetic circuit formed of a plurality of exclusive-ORs depending on the generator polynomial G(X). The parallel data input from the standard bus and the parallel data in the register 25 to which the remainder equation R(X) is set are input into the ALU 24 and the ALU performs an arithmetic operation before the following data arrives from the standard bus to set the results to the register 25 again. The above process is repeated until the final data arrives to set the CRC codes to the register 25.

[0031]

The error control device controlling section 26 performs the changeover of a selector in the error control device 1 and the input-output control of data based on the control signal of the standard bus and the signal of the bus dedicated for CRC error detection. The bus control signal generating section 27 performs the output control of the signal line on the standard bus in the transfer of data with the CRC code.

[0032]

A comparator 29 in the error control device 1 on the data receiving side checks if the received data in the register 25 is a certain fixed value. If the data is not a certain fixed value, an error should be

produced. A necessary process for the error is conducted by the bus control signal generating section 27 and the control signal generating section 28 dedicated for CRC error detection.

[0033]

Figure 5 shows the timing chart for the transfer of data with the CRC codes. The CRC code is formed of generally 16 bits or 32 bits. As shown in Figure 5, the bit number of the CRC code is met to the data width of the bus, which always adds only one cycle to the transfer of the CRC code irrespective of the quantity of the transfer data.

[0034]

The bit number of the CRC code may be integral multiples of the data width of the bus. In this case, several cycles are required to transfer the CRC code, however, the quantity of data to be handled in error detection can be substantially increased. For example, the increase of the CRC code to 32 bits from 16 bits enables the increase of the quantity of transmission data which can be handled in error detection of 2 bits or less to 268 Mbytes from 4 Kbytes.

[0035]

The number of cycles required for the transfer of the CRC code is several cycles at the most, which does not cause any problem for cases where an enormous quantity of data is handled in burst transfer and block transfer, however, transfer efficiency is lowered when a single transfer continues.

[0036]

A method is available of adding the CRC code according to the quantity of data when there is little probability of errors being generated in a small quantity of data. The CRC code is not added in a single transfer by taking advantage of the signal showing burst

transfer provided on the standard bus. As described above, as is the case where the error control device 1 on the bus slave side is received transfer from bus master without the error control device 1, the error control device 1 on the bus slave side does not perform error detection because there is no communication from the error control device 1 of the bus master.

[0037]

The embodiment in Figure 1 uses the standard bus and the standard I/O attached thereto as it is, so that restrictions are placed on an error detection report means, or transfer time is extended a little. Figure 6 shows an embodiment of a high reliability and performance system to improve reliability and reduce transfer time to the shortest possible level.

[0038]

In Figure 6, reference numeral 31 denotes an error control device in which a dedicated communication control line is added to the error control device 1 in Figure 1; 2, a standard bus without a parity bit method; 33, CPU managing the entire system provided with the dedicated communication control line which communicates with the error control device 31; 34, main storage; 35, input-output device provided with the dedicated communication control line which communicates with the error control device 31; 36, dedicated bus connected only to the error control device 31; and 37, dedicated communication control line handshaking the error control device 31.

[0039]

The error control device 31 is substantially the same in internal configuration as that in Figure 4 but is different in that the block corresponding to the control signal generating section 28 dedicated

for CRC error detection controls the dedicated bus 26 and the dedicated handshake signal 37 instead of the dedicated bus 6.

[0040]

In the embodiment shown in Figure 6, as is the case with Figure 1, an error detection processing is not performed in transfer with the standard I/O which does not place the error control device 31. On the other hand, when the error detection processing is performed in transfer between the dedicated devices which place the error control device 31, a bus is released immediately after the CRC code is transferred on the standard bus and the dedicated bus 36 and the dedicated handshake signal 37 are used as error detection report means.

[0041]

Furthermore, the standard bus 2 is combined with the dedicated bus 36 to form one bus provided with the CRC method, and the error control device 31 is incorporated into each device to realize a dedicated CPU 43, dedicated main storage 44 and dedicated input-output device 45.

[0042]

The embodiment in Figure 6 is characterized in that (1) an I/O which does not need error control by the CRC method, in other words, an I/O which does not require high reliability may use the standard I/O, and (2) even when error detection processing is performed by the error control device 31, the use of the dedicated communication control line 37 in the error detection report means does not influence transfer time on the standard bus.

[0043]

Thus, the bus communication means provided with the CRC method has a plurality of means to be realized.

[0044]

In the present embodiment, the use of the CRC method used in communication networks as error detection means for improving reliability of bus communication in a computer system using the standard bus without the parity bit method enables the construction of highly reliable system using the standard bus excellent in cost performance.

[0045]

According to the present invention, the use of the bus provided with the CRC method as error detection means for improving reliability of bus communication in the computer system enables the construction of highly reliable system handling an enormous amount of data.

[0046]

Furthermore, also in a computer system using the standard bus without the CRC method, an error control device with a CRC code generator and an error detector is interposed between a standard bus and the adapters and memories which are attached to the standard bus to add CRC codes to the end of the data transmission to detect errors, which allows the construction of a highly reliable system to which many versatile adaptors of the standard bus are made available.

[Brief Description of the Drawings]

[Figure 1]

Figure 1 shows an example of configuration of the computer system which has the bus communication means according to the embodiment of the present invention and is provided with the standard bus and standard I/O.

[Figure 2]

Figure 2 show one example of data format of the bus with parity bit method.

[Figure 3]

Figure 3 shows one embodiment of the CRC used in communication network

[Figure 4]

Figure 4 shows a functional block diagram of the error control device 1.

[Figure 5]

Figure 5 shows the timing chart for the transfer of data with the CRC codes.

[Figure 6]

Figure 6 shows an example of configuration of the computer system which has the bus communication means according to the embodiment of the present invention and is provided with dedicated CPU, dedicated main storage and dedicated I/O in addition to the standard bus and standard I/O.

[Description of Symbols]

1 ... Error control device with CRC code generator and error detector

2 ... Standard bus without parity bit method

3 ... CPU managing the entire computer system

4 ... Main storage

5 ... Input-output device

6 ... Dedicated bus connected only to the error control device 1

11 ... Shift register

12 ... EX-OR processor

13 ... Changeover switch for switching operation output results to destination

22 ... Data line out of the signal lines of the standard bus 2

23 ... Signal line except the data line 22 in the standard bus 2

24 ... ALU realized by operation circuit configuration depending on generator polynomial G(X)

25 ... Register to which remainder equation R(X) is set

26 ... Error control device controlling section for controlling each function in the error control circuit 1

27 ... Bus control signal generating section for controlling the output timing of the control signal of the standard bus when data with CRC code is transferred

28 ... Control signal generating section dedicated for CRC error detection which processes signal line of the dedicated bus 6

29 ... Comparator checking if all bits forming the register 25 are zero

31 ... Error control device provided with CRC code generator and error detector

33 ... CPU managing the entire computer

34 ... Main storage

35 ... Input-output device dedicated for the bus provided with the error detection method

36 ... Bus connected only to the error control device 31

37 ... Dedicated communication control line handshaking the error control device 31

43 ... CPU with the function of the error control device 31

44 ... Main storage with the function of the error control device 31

45 . . . Input-output device with the function of the error control device 31

Figure 2

#1 ORDER OF DATA TRANSFER

#2 ODD PARITY

#3 ERROR DETECTION

#4 COMPOSING ELEMENTS OF 8 BIT DATA (0 OR 1)

#5 ODD PARITY (TO BE SET SO THAT NUMBER OF 1 IN 9 BITS OF b_0 to p IS ODD NUMBER)

Figure 3

#1 REMAINDER CALCULATION

#2 REMAINDER OUTPUT

#3 SELECTOR

#4 SELECTION SIGNAL

Figure 4

#1 SELECTOR

#2 COMPARATOR

#3 ERROR CONTROL DEVICE CONTROLLING SECTION

#4 BUS CONTROL SIGNAL GENERATING SECTION

#5 CONTROL SIGNAL GENERATING SECTION DEDICATED FOR CRC ERROR DETECTION

Figure 5

#1 SIGNAL ON BUS

#2 DATA TRANSFER PERIOD

#3 CRC TRANSFER AND PROCESSING TIME

7

能にしている。

【００４５】

【発明の効果】本発明によれば、計算機システム内のバス通信の信頼性向上を図るための誤り検出手段として、ＣＲＣ方式を備えたバスを採用することにより、膨大な量のデータを扱う高信頼性システムの構築を可能にする。

【００４６】また、ＣＲＣ方式を持たない標準バスを用いた計算機システムにおいても、標準バスと、その標準バスに付く各アダプタ及びメモリ等の間に、ＣＲＣ符号生成器と誤り検出器を備えた誤り制御装置を置くことにより、データ転送の末尾にＣＲＣ符号を付けて、誤り検出のできるバス通信手段を実現することができる。この結果、標準バスの持つ豊富な汎用アダプタを利用できる高信頼性システムを構築することができる。

【図面の簡単な説明】

【図１】本発明の実施例であるバス通信手段を持ち、標準バス及び標準Ｉ／Ｏを備えた計算機システムの構成例を示す図である。

【図２】パリティビット方式を持つバスのデータ形式の一例を示す図である。

【図３】通信ネットワークで用いられるＣＲＣの一実施例を示す図である。

【図４】誤り制御装置１の機能ブロック図である。

【図５】ＣＲＣ符号を付加したデータ転送のタイミングチャートである。

【図６】本発明の実施例であるバス通信手段を持ち、標準バス及び標準Ｉ／Ｏの他に専用ｃｐｕ、専用主記憶装置及び専用Ｉ／Ｏを備えた計算機システムの構成例を示す図である。

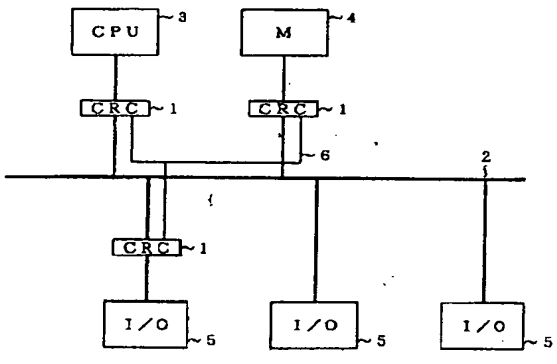
8

【符号の説明】

１…ＣＲＣ符号生成器及び誤り検出器を備えた誤り制御装置、２…パリティビット方式を持たない標準バス、３…計算機システム全体を管理するＣＰＵ、４…主記憶装置、５…入出力装置、６…誤り制御装置１のみが接続する専用バス、１１…シフトレジスタ、１２…ＥＸ－ＯＲ演算器、１３…演算結果出力先の切り替えスイッチ、２２…標準バス２の信号線のうちのデータ線、２３…標準バス２からデータ線２２を除いた信号線、２４…生成多項式Ｇ（Ｘ）に依存する演算回路構成で実現されるＡＬＵ、２５…剰余式Ｒ（Ｘ）がセットされるレジスタ、２６…誤り制御回路１内の各機能を制御する誤り制御装置制御部、２７…ＣＲＣ符号を付けたデータ転送を行うときに標準バスの制御信号の出力タイミングを制御するバス制御信号生成部、２８…専用バス６の信号線を処理するＣＲＣ誤り検出専用制御信号生成部、２９…レジスタ２５を構成する全ビットが０かどうかチェックする比較器、３１…ＣＲＣ符号生成器及び誤り検出器を備えた誤り制御装置、３３…計算機システム全体を管理するＣＰＵ、３４…主記憶装置、３５…誤り検出方式を備えたバス専用の入出力装置、３６…誤り制御装置３１のみが接続する専用バス、３７…誤り制御装置３１とのハンドシェークを行う専用通信制御線、４３…誤り制御装置３１の機能を備えたＣＰＵ、４４…誤り制御装置３１の機能を備えた主記憶装置、４５…誤り制御装置３１の機能を備えた入出力装置。

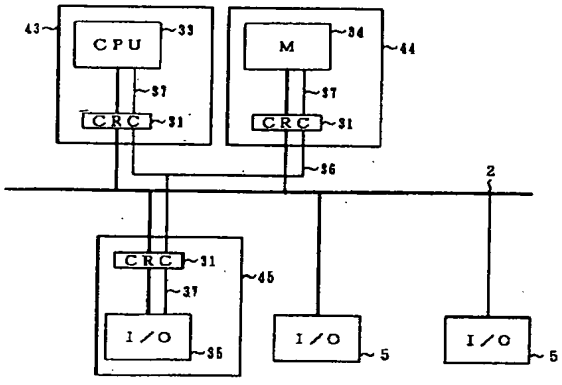
【図１】 FIG. 1

図 1



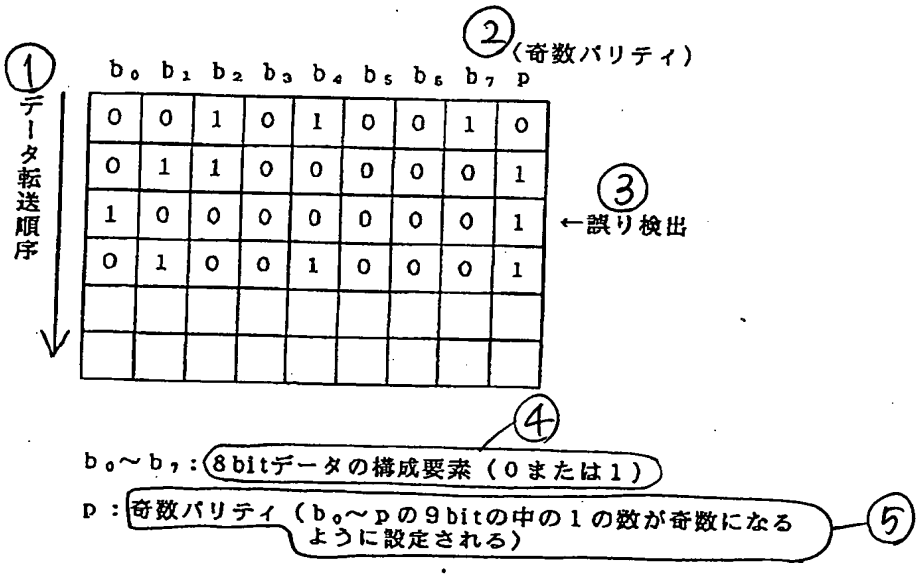
【図６】 FIG. 6

図 6



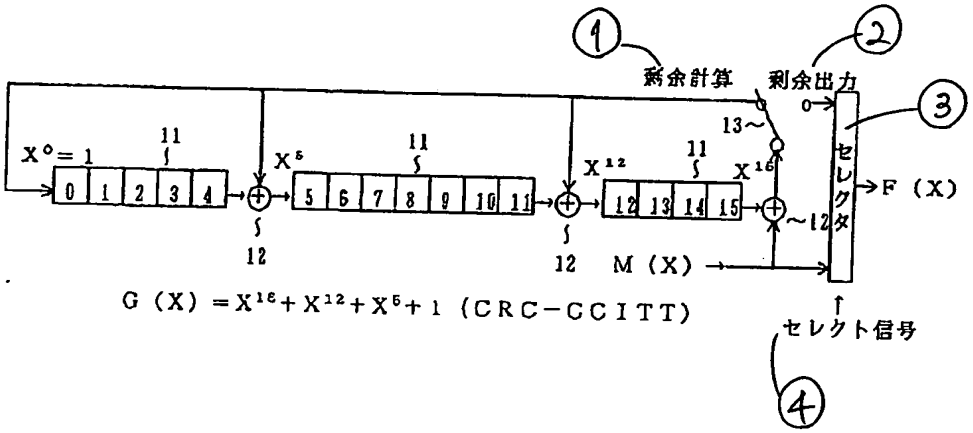
【図2】 FIG. 2

図 2



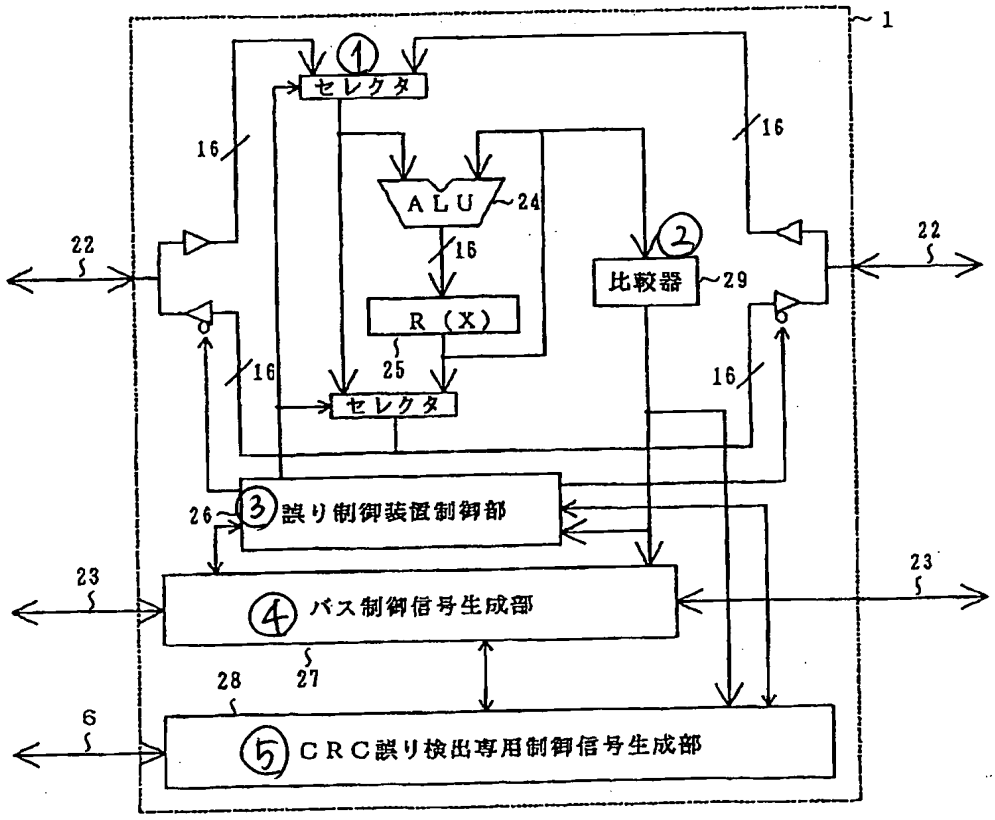
【図3】 FIG. 3

図 3



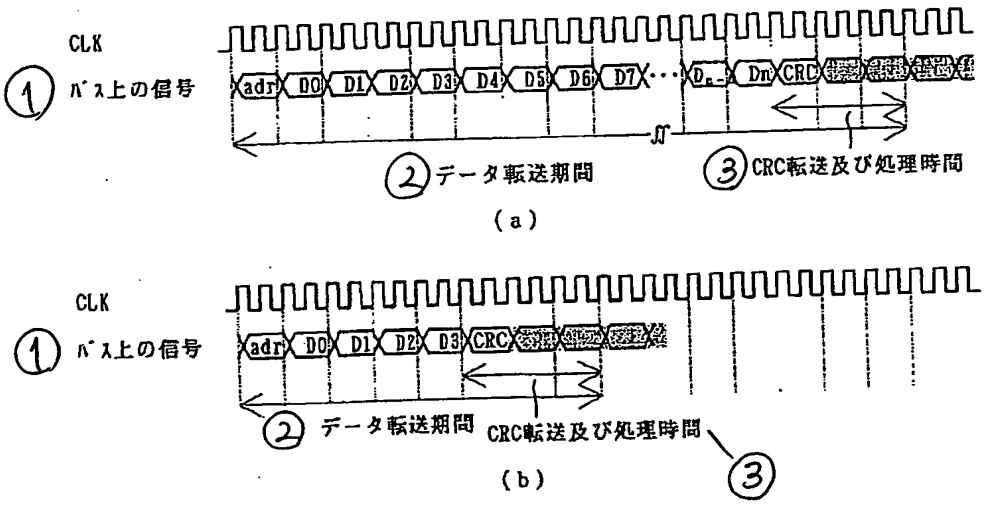
【図4】 FIG. 4

図 4


1
①
セレクタ
16
16
ALU
24
16
②
比較器
29
22
22
R（X）
25
16
16
セレクタ
26
③誤り制御装置制御部
23
23
④バス制御信号生成部
27
28
6
⑤CRC誤り検出専用制御信号生成部

【図5】 FIG.5

図 5



フロントページの続き

(72)発明者　小倉　敏彦
横浜市戸塚区吉田町292番地株式会社日立製作所マイクロエレクトロニクス機器開発研究所内

(72)発明者　篠崎　雅継
神奈川県海老名市下今泉810番地株式会社日立製作所オフィスシステム設計開発センタ内